Refine Search

Search Results -

Terms	Documents
(storage or memory or disk or disc) same ((intercontroller or (inter adj1 controller)) same link)	37

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L1	(storage or memory or disk or disc) same ((intercontroller or (inter adj1 controller)) same link)	37	L1

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Search Results -

Terms	Documents
(370/363 |370/452 |710/5 |710/36 |710/62 |710/63 |710/100 |710/300 |711/113 |711/114 |711/130 |711/118 |711/112 |711/148 |711/141 |700/2 |714/5 |714/7 |714/9).ccls.	12170

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	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L2	710/5,36,62,63,100,300;711/113,114,130,118,112,148,141;714/5,7,9;700/2;370/363,452.ccls.	12170	L2
L1	(storage or memory or disk or disc) same ((intercontroller or (inter adj1 controller)) same link)	37	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L2	23

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
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- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L3

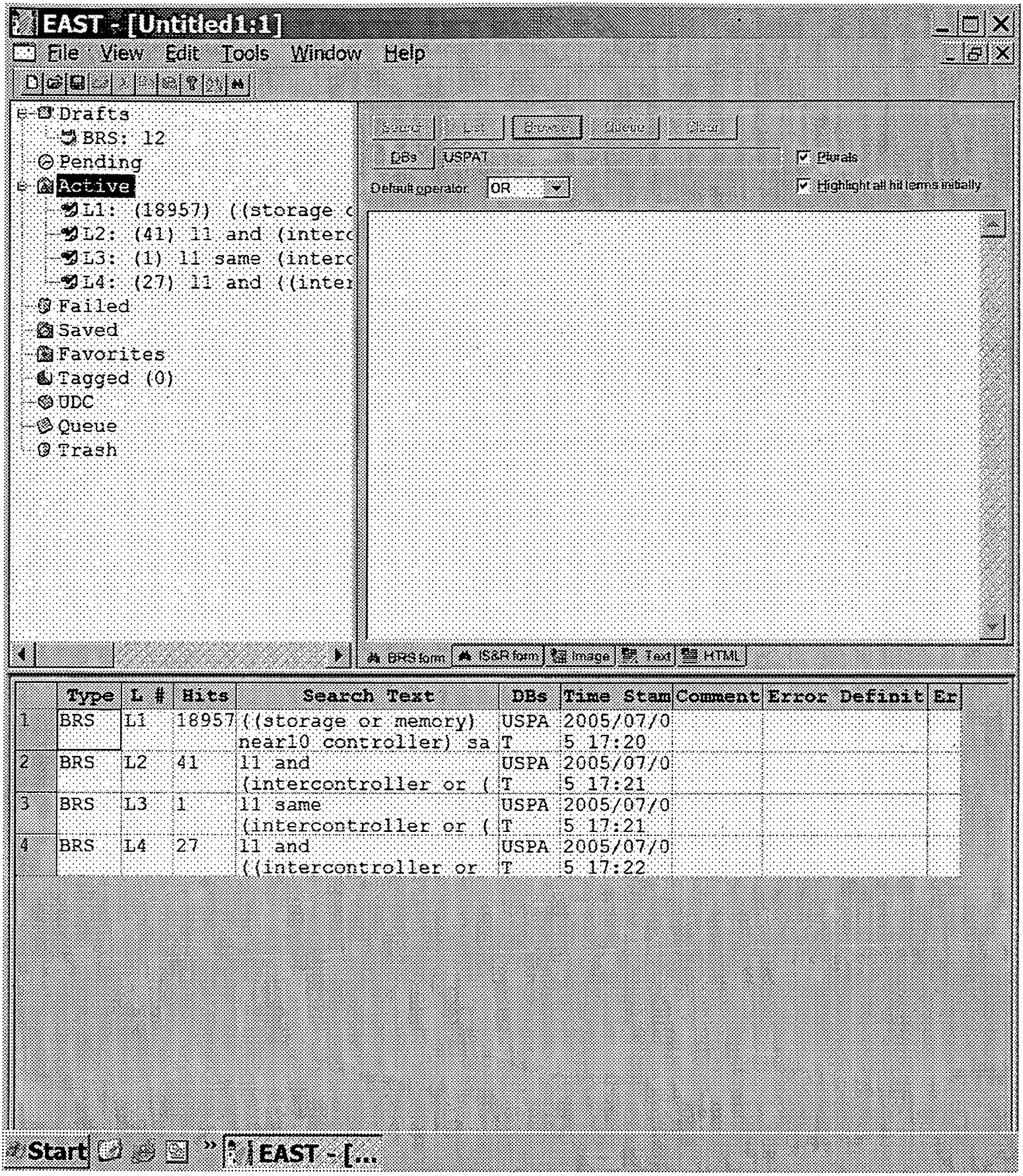
Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, July 07, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	l1 and L2	23	L3
L2	710/5,36,62,63,100,300;711/113,114,130,118,112,148,141;714/5,7,9;700/2;370/363,452.ccls.	12170	L2
L1	(storage or memory or disk or disc) same ((intercontroller or (inter adj1 controller)) same link)	37	L1

END OF SEARCH HISTORY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3 BRS L3 1 l1 same (intercontroller or (USPAT 2005/07/05 17:21
4 BRS L4 27 l1 and ((intercontroller or USPAT 2005/07/05 17:22
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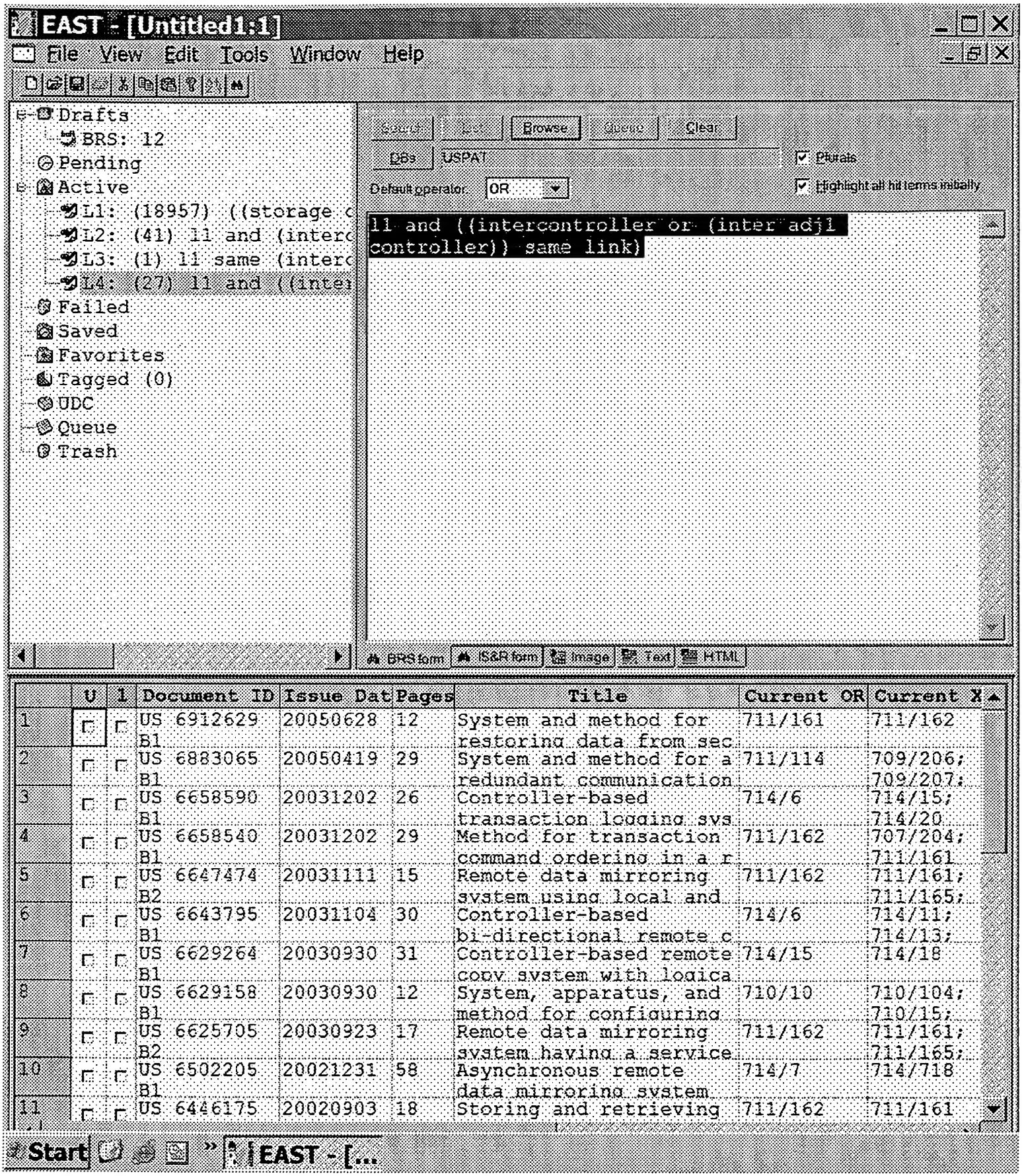
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1 US 6912629 B1 20050628 12 System and method for restoring data from sec 711/161 711/162
2 US 6883065 B1 20050419 29 System and method for a redundant communication 711/114 709/206; 709/207;
3 US 6658590 B1 20031202 26 Controller-based transaction logging sys 714/6 714/15; 714/20
4 US 6658540 B1 20031202 29 Method for transaction command ordering in a r 711/162 707/204; 711/161
5 US 6647474 B2 20031111 15 Remote data mirroring system using local and 711/162 711/161; 711/165;
6 US 6643795 B1 20031104 30 Controller-based bi-directional remote c 714/6 714/11; 714/13;
7 US 6629264 B1 20030930 31 Controller-based remote copy system with logica 714/15 714/18
8 US 6629158 B1 20030930 12 System, apparatus, and method for configuring 710/10 710/104; 710/15;
9 US 6625705 B2 20030923 17 Remote data mirroring system having a service 711/162 711/161; 711/165;
10 US 6502205 B1 20021231 58 Asynchronous remote data mirroring system 714/7 714/718
11 US 6446175 20020903 18 Storing and retrieving 711/162 711/161
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EAST - [...

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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(intercontroller or (inter controller)<in>metadata) <and> (link<in>metadata)

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1. **A four station controller area network**
Boyce, C.R.;
Vehicle Networks for Multiplexing and Data Communication, IEE Colloquium on
19 Dec 1988 Page(s):9/1 - 9/7
AbstractPlus | Full Text: PDF(196 KB) IEE CNF

2. **Resource management in an integrated optical network**
Sohraby, K.; Zhensheng Zhang; Xiaowen Chu; Bo Li;
Selected Areas in Communications, IEEE Journal on
Volume 21, Issue 7, Sept. 2003 Page(s):1052 - 1062
AbstractPlus | References | Full Text: PDF(490 KB) IEEE JNL

Resource management in an integrated optical network

Sohraby, K. Zhensheng Zhang Xiaowen Chu Bo Li
Bell Labs., Holmdel, NJ, USA

This paper appears in: **Selected Areas in Communications, IEEE Journal on**
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On page(s): 1052 - 1062
ISSN: 0733-8716
INSPEC Accession Number:7737648
DOI: 10.1109/JSAC.2003.815978
Posted online: 2003-09-08 14:27:55.0

Abstract
We propose a novel integrated optical network switching architecture. The proposal offers an approach to signaling for the purpose of transport on an all-optical network of optical and nonoptical legacy network traffic. In order to provide effective end-to-end control and efficient transport services, new signaling and control techniques are required. Standard organizations such as Optical Interworking Forum (OIF) and Internet Engineering Task Force have developed interface methods between client and transport networks, as well as signaling processes for resource allocation. We propose a network controller, which implements interfaces for such integration in the intermediate future, as well as provides a feasible path for the long-term objective of all optical networking. Performance and capacity issues for these systems introduce new dimensions to the existing set of networking problems, since optical paths can now be set up in real-time. There are two main contributions in this paper: (1) functional composition of a network controller, which translates legacy signaling to optical connection signaling and path establishment and (2) determining when to issue an optical connection request based on the current network conditions such as **link** utilization, so that the integrated optical network can operate efficiently. Analytical approximations, as well as simulation results for call blocking performance are also presented.

Index Terms
Inspec

Controlled Indexing
optical fibre networks standardisation telecommunication congestion control telecommunication control telecommunication network management telecommunication signalling telecommunication traffic wavelength division multiplexing

Non-controlled Indexing
DWDM IETF Internet Engineering Task Force Optical Interworking Forum all-optical network analytical approximations call blocking performance client networks dense wavelength division multiplexing efficient transport services end-to-end control integrated optical network integrated optical network switching architecture interface methods legacy signaling link utilization network conditions network controller network performance network signaling nonoptical legacy network traffic optical connection request optical connection signaling optical legacy network traffic path establishment real-time optical paths resource allocation resource management simulation

results standard organizations transport networks

Author Keywords

Not Available

References

1 *Internet Protocol Device Control, Revision 0.17*, 2000.

2 J. T.Moy, *OSPF Anatomy of an Internet Routing Protocol* Reading, MA: Addison-Wesley, 1998.
[Buy Via Ask*IEEE]

3 K. Sohraby, M. Fatehi, V. Lawrence, and M. Wilson, "Network architecture for an all-optical internet," *NFOEC 2000* Denver, CO.
[Buy Via Ask*IEEE]

4 *User Network Interface (UNI) 1.0 Signaling Specification* Fremont, CA: Optical Interworking Forum, Contribution OIF2000.125.7, 2001.

5 D. Benzamin, R. Trudel, S. Shew, and E. Kus, "Optical services over the intelligent optical network," *IEEE Commun. Mag.*, pp. 73-78, Sept. 2001.
Abstract | Full Text: PDF (2051KB)

6 U. Schoen *et al.*, "Convergence between public switching and the internet," *IEEE Commun. Mag.*, pp. 50-65, Jan. 1998.
Abstract | Full Text: PDF (2500KB)

7 C. Low, "Integrating communications services," *IEEE Commun. Mag.*, pp. 164-169, June 1997.
Abstract | Full Text: PDF (1448KB)

8 D. Jeske, B. Samadi, K. Sohraby, Y.-T.Wang, and Q.Zhang, "QoS with an edge-based call admission control in IP networks," presented at the *Proc. Networking* Pisa, Italy, May 2002.
[Buy Via Ask*IEEE]

9 K. Sohraby and M. Fatehi, "Digital container: A mechanism for heterogeneous traffic transport over an all-optical network," *Opt. Networks*, vol. 2, no. 3, pp. 45-57, May/June 2001.
[Buy Via Ask*IEEE]

10 G. R.Ash, *Dynamic Routing in Telecommunications Networks* New York: McGraw-Hill, 1997.
[Buy Via Ask*IEEE]

11 K. Sohraby and K. Ryan, "An architecture for signaling, switching, and control in optical networks," presented at the *6th World Multiconference on Systematics, Cybernetics, and Informatics (SCI)* Orlando, FL, July 2002.
[Buy Via Ask*IEEE]

12 J.Bellamy, *Digital Telephony*, 2nd ed. New York: Wiley, 1990.
[Buy Via Ask*IEEE]

13 [online] Available: http://www.lucent.com.

14 Z. Zhang and X. Liu, "Network models for IP over optical networks," *Opt. Network Mag.*, vol. 1, no. 4, pp. 12-14, Oct. 2000.
[Buy Via Ask*IEEE]

15 *Generalized Multi-Protocol Label Switching (GMPLS) Architecture*, draft-ietf-ccamp-gmpls-architecture-03.txt, work in progress.

16 Z. Zhang, D. Guo, L. Zhang, and J. Fu, "Lightpath routings in intelligent optical networks," *IEEE Network*, vol. 15, pp. 28-35, July/Aug. 2001.
Abstract | Full Text: PDF (1812KB)

17 K. Thompson *et al.*, "Wide area internet traffic patterns and characteristics," *IEEE Network*, vol. 11, pp. 10-23, Nov. 1997.
Abstract | Full Text: PDF (4912KB)

18 R. A. Lakshmi, "The lucent technologies softswitch: Realizing the promise of convergence," *Bell Labs Tech. J.*, vol. V24, no. 2, Apr.–

June 1999.

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Citing Documents

No citing documents available on IEEE Xplore.

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US006643795B1

(12) **United States Patent**
Sicola et al.

(10) Patent No.: US 6,643,795 B1
(45) Date of Patent: Nov. 4, 2003

(54) **CONTROLLER-BASED BI-DIRECTIONAL REMOTE COPY SYSTEM WITH STORAGE SITE FAILOVER CAPABILITY**

(75) Inventors: Stephen J. Sicola, Monument, CO (US); Susan G. Elkington, Colorado Springs, CO (US)

(73) Assignee: Hewlett-Packard Development Company, L.P., Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/538,680

(22) Filed: Mar. 30, 2000

(51) Int. Cl.[7] G06F 11/00

(52) U.S. Cl. 714/6; 714/7; 714/11; 714/13

(58) Field of Search 714/6, 11, 5, 4, 714/7, 13

(56) References Cited

U.S. PATENT DOCUMENTS

5,274,645	A	12/1993	Idleman et al.	371/12.1
5,544,347	A *	8/1996	Yanai et al.	711/162
5,570,360	A *	11/1996	Kotzur et al.	714/38
5,768,623	A *	6/1998	Judd et al.	710/17
5,771,344	A *	6/1998	Chen et al.	714/7
5,790,775	A	8/1998	Marks et al.	395/182.05
5,870,537	A *	2/1999	Kern et al.	711/162
5,933,653	A *	8/1999	Obi	710/6
6,009,542	A *	12/1999	Beardsley et al.	714/5
6,167,531	A *	12/2000	Slivinski	714/13
6,401,170	B1 *	6/2002	Griffith et al.	714/7

OTHER PUBLICATIONS

Sicola, Stephen J. et al., U.S. patent application, Fault Tolerant Storage Controller Utilizing Tightly Coupled Dual Controller Modules, Ser. No. 08/071,710, filed Jun. 4, 1993, pp. 1-90.

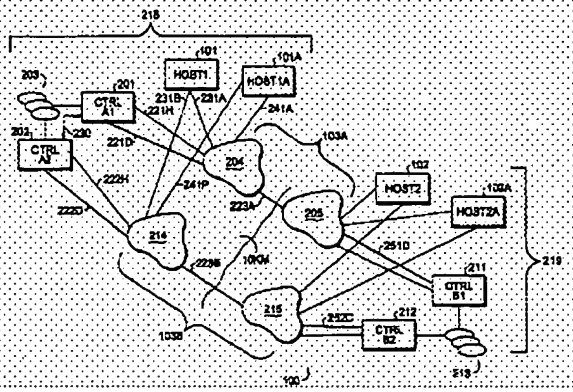
* cited by examiner

Primary Examiner—Robert Beausoliel
Assistant Examiner—Marc Duncan

(57) **ABSTRACT**

A data replication system having a redundant configuration including dual Fibre Channel fabric links interconnecting each of the components of two data storage sites, wherein each site comprises a host computer and associated data storage array, with redundant array controllers and adapters. The system includes the capability of simultaneous bi-directional remote data replication which permits the system to operate in an "extended cluster" mode, as if each of the remote storage arrays were 'local' relative to the respective remote host. The system further includes the concept of 'home' and 'alternate' storage nodes, which provide for automatic node failover from a primary to a designated alternate node, without necessitating re-booting of the remote node. Write data transfers are potentially host recoverable at both sites upon failure of controllers at one site, the host re-issues the same write on other site.

17 Claims, 18 Drawing Sheets



US-PAT-NO: 6643795

DOCUMENT-IDENTIFIER: US 6643795 B1

TITLE: Controller-based bi-directional remote copy system with storage site failover capability

---------- KWIC ----------

Brief Summary Text - BSTX (8):

U.S. Pat. No. 5,274,645 (Dec. 28, 1993), to Idleman et al. discloses a dual-active configuration of storage controllers capable of performing failover without the direct involvement of the host. However, the direction taken by Idleman requires a multi-level storage controller implementation. Each controller in the dual-redundant pair includes a two-level hierarchy of controllers. When the first level or host-interface controller of the first controller detects the failure of the second level or device interface controller of the second controller, it re-configurss the data path such that the data is directed to the functioning second level controller of the second controller. In conjunction, a switching circuit re-configures the controller-device interconnections, thereby permitting the host to access the storage devices originally connected to the failed second level controller through the operating second level controller of the second controller. Thus, the presence of the first level controllers serves to isolate the host computer from the failover operation, but this isolation is obtained at added controller cost and complexity.

Brief Summary Text - BSTX (10):

U.S. patent application Ser. No. 08/071,710 to Sicola et al., describes a dual-active, redundant storage controller configuration in which each storage controller communicates directly with the host and its own attached devices, the access of which is shared with the other controller. Thus, a failover operation may be executed by one of the storage controller without the assistance of an intermediary controller and without the physical reconfiguration of the data path at the device interface.

Detailed Description Text - DETX (15):

The array controllers 201/202 and 211/212 employed by the present system 100 have two host ports 109 per array controller, for a total of four connections (ports) per pair in the dual redundant configuration of FIG. 3. Each host port 109 preferably has an optical attachment to the switched fabric, for example, a Gigabit Link Module (`GLM`) interface at the controller, which connects to a Gigabit Converter (`GBIC`) module comprising the switch interface port 107. Switch interconnection ports 306 also preferably comprise GBIC modules. Each pair of array controllers 201/202 and 211/212 (and associated storage array) is also called a storage node (e.g., 301 and 302), and has a unique Fibre Channel Node Identifier. As shown in FIG. 3, array controller pair A1/A2 comprise storage node 301, and array controller pair B1/B2 comprise storage node 302.

US-PAT-NO: 6237028

DOCUMENT-IDENTIFIER: US 6237028 B1

TITLE: Host central processor with associated controller to capture a selected one of a number of memory units via path control commands

---------- KWIC ----------

Brief Summary Text - BSTX (4):
Workers are also familiar with the practice of associating one or several host central processors (CPUs) with an array of memory units via intermediate controllers (e.g. see U.S. Pat. No. 4,982,324, 4,413,317, 3,889,237, 4,183,084, 3,623,014). And, today, it is not uncommon to operatively associate an array of peripheral storage units with a host computer via an appropriate controller device. FIG. 1 schematically suggests this for a host H and a number of like memory units D, connectible to H via a controller unit C, including suitable interfaces IF, IF' (e.g. see ports 1-4, each connected to a respective, like-numbered drive-port).

Brief Summary Text - BSTX (7):
Now, it may become desirable to mediate the competition between two host-computers to "capture" a selected memory unit (e.g. drive), using certain mediation means. Such a mediation means is the "Shared Memory Interface" (Smi) indicated in FIG. 3, shown in operative relation with eight dual-ported disk drives D0-D7 and a pair of host/controller arrays: host A15 with Controller A and host A17 with Controller B, plus suitable controller inter-faces, IPI-2, IPI-3. Workers should realize that mediation means Smi provides a communication link that allows one controller to request, or transmit, information to, or from, the other controller--here via what may be called "direct memory access" (DMA) something that requires special interfaces [e.g. additional special hardware, as "shared memory", SM, and associated interfaces I-A, I-B, (memory typically a dedicated random access memory RAM) and special software]. Shared memory, SM, also functions as a common storage unit that can be used to maintain "data path control"; i.e. allow/disallow a host to write/read information to/from a selected disk drive.

Brief Summary Text - BSTX (14):
A salient feature of this "Natural Linking" is that it operates "Controller-to-Controller", using only a disk drive as its link, i.e. linking via means which are already part of the system (e.g. here only via a disk drive normally coupled to a M-9730 Controller, plus the "standard" IPI-2 interface normally used by this Controller). That is, here, the inter-controller linkage is "natural", using an already-present disk drive unit via an IPI-2 interface which is normally used for disk control or read/write commands, This way, one controller can now, use its normal (natural) interface to communicate with the other controller, --both controllers being coupled to the two ports of each

US006237028B1

(12) **United States Patent**
Jackson

(10) Patent No.: **US 6,237,028 B1**
(45) Date of Patent: ***May 22, 2001**

(54) **HOST CENTRAL PROCESSOR WITH ASSOCIATED CONTROLLER TO CAPTURE A SELECTED ONE OF A NUMBER OF MEMORY UNITS VIA PATH CONTROL COMMANDS**

(75) Inventor: **Gary Edward Jackson**, Lake Forest, CA (US)

(73) Assignee: **Unisys Corporation**, Blue Bell, PA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/152,692**

(22) Filed: **Sep. 2, 1998**

Related U.S. Application Data

(62) Division of application No. 08/650,665, filed on May 2, 1997, now Pat. No. 5,812,782, which is a division of application No. 08/215,662, filed on Mar. 21, 1994, now Pat. No. 5,630,169, which is a division of application No. 07/949,967, filed on Sep. 24, 1992, now Pat. No. 5,594,926.

(51) Int. Cl.[7] G06F 12/02; G06F 13/14

(52) U.S. Cl. 709/214; 709/210; 710/5; 710/36

(58) Field of Search 709/214, 210; 710/5, 36

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,747,043	*	5/1988	Rodman	364/200
4,747,047	*	5/1988	Coogan et al.	364/200
4,849,190	*	10/1989	Hamilton et al.	364/900
5,060,140	*	10/1991	Brown et al.	364/200

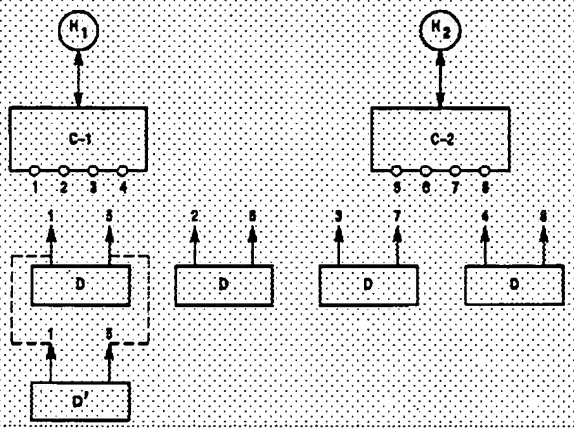
* cited by examiner

Primary Examiner—Thomas C. Lee
Assistant Examiner—Rehana Perveen
(74) *Attorney, Agent, or Firm*—Mark T. Starr

(57) **ABSTRACT**

A pair of data processing systems, each of the data processing system having a host central processor and an associated controller including memory, both of the data processing systems to be cooperatively associated with a number of disk drive memory units, each of the disk drive memory unit coupled to both said controllers. Either one of the host central processors can appropriate any one of the disk drive memory units as a selected disk drive memory unit by propagating path-control-data to the memory in both of the controllers and in the selected disk drive memory unit.

3 Claims, 7 Drawing Sheets



US-PAT-NO: 5630169

DOCUMENT-IDENTIFIER: US 5630169 A

TITLE: Apparatus for a host central processor with associated controller to capture a selected one of a number of memory units via path control commands

---------- KWIC ---------

Brief Summary Text - BSTX (4):

Workers are also familiar with the practice of associating one or several host central processors (CPUs) with an array of memory units via intermediate controllers (e.g. see U.S. Pat. Nos. 4,962,324, 4,413,317, 3,889,237, 4,183,084, 3,623,014). And, today, it is not uncommon to operatively associate an array of peripheral storage units with a host computer via an appropriate controller device. FIG. 1 schematically suggests this for a host H and a number of like memory units D, connectible to H via a controller unit C, including suitable interfaces IF, IF' (e.g. see ports 1-4, each connected to a respective, like-numbered drive-port).

Brief Summary Text - BSTX (7):

Now, it may become desirable to mediate the competition between two host-computers to "capture" a selected memory unit (e.g. drive), using certain mediation means. Such a mediation means is the "Shared Memory Interface" (SMi) indicated in FIG. 3, shown in operative relation with eight dual-ported disk drives D0-D7 and a pair of host/controller arrays: host A16 with Controller A and host A17 with Controller B, plus suitable controller inter-faces, IPI-2, IPI-3. Workers should realize that mediation means SMi provides a communication link that allows one controller to request, or transmit, information to, or from, the other controller--here via what may be called "direct memory access" (DMA) something that requires special interfaces (e.g. additional special hardware, as "shared memory", SM, and associated interfaces I-A, I-B, (memory typically a dedicated random access memory RAM) and special software]. Shared memory, SM, also functions as a common storage unit that can be used to maintain "data path control": i.e. allow/disallow a host to write/read information to/from a selected disk drive.

Brief Summary Text - BSTX (14):

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US005630169A

United States Patent [19]

Jackson

[11] Patent Number: 5,630,169

[45] Date of Patent: *May 13, 1997

[54] APPARATUS FOR A HOST CENTRAL PROCESSOR WITH ASSOCIATED CONTROLLER TO CAPTURE A SELECTED ONE OF A NUMBER OF MEMORY UNITS VIA PATH CONTROL COMMANDS

[75] Inventor: Gary E. Jackson, Lake Forest, Calif.

[73] Assignee: Unisys Corporation, Blue Bell, Pa.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,504,926.

[21] Appl. No.: 625,662

[22] Filed: Mar. 29, 1996

Related U.S. Application Data

[62] Division of Ser. No. 949,597, Sep. 24, 1992, Pat. No. 5,504,926.

[51] Int. Cl.[6] G06F 12/02; G06F 13/14

[52] U.S. Cl. 395/825; 395/856; 395/475; 395/439; 395/200.01

[58] Field of Search 395/825, 856, 395/475, 200.01, 725, 439

[56] References Cited

U.S. PATENT DOCUMENTS

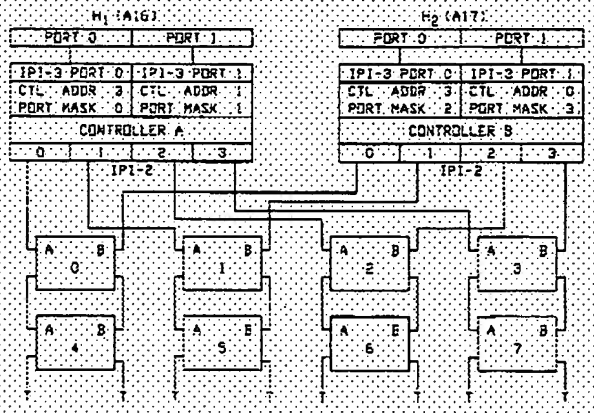
4,455,621	6/1984	Pilley et al.	364/900
4,747,043	5/1988	Rodman	364/200
4,759,010	7/1988	Mizuno et al.	370/58
5,060,140	10/1991	Brown et al.	364/200
5,261,073	11/1993	Siegel	395/425
5,295,247	3/1994	Chang et al.	395/325
5,325,488	6/1994	Carson et al.	395/275

Primary Examiner—Thomas C. Lee
Assistant Examiner—Rehana Perveen Rifkin
Attorney, Agent, or Firm—John T. McCormack; Mark T. Starr

[57] ABSTRACT

A pair of data processing systems, each of the data processing system having a host central processor and an associated controller including memory, both of the data processing systems to be cooperatively associated with a number of disk drive memory units, each of the disk drive memory units coupled to both said controllers. Either one of the host central processors can appropriate any one of the disk drive memory units as a selected disk drive memory unit by propagating path-control-data to the memory in both of the controllers and in the selected disk drive memory unit.

3 Claims, 7 Drawing Sheets



US-PAT-NO: 4791629

DOCUMENT-IDENTIFIER: US 4791629 A

TITLE: Communications switching system

---------- KWIC ----------

Detailed Description Text - DETX (47):
Data values are stored into SE buffer memory which are read by the SEP 64 and stored into frame space. These values include the next intercontroller corresponding address, the link input and output channel pointer, and data values stored in the IEOFIFO. Values in the IEOFIFO can be any values that are in frame space including corresponding addresses, time slot registers, link control and codec enable etc.

Detailed Description Text - DETX (151):
The controller provides a means of controlling communication between the Xbus 23 and the digital stations or analog interfaces to which each controller is coupled. Each controller provides storage for incoming and outgoing data as well as switching services for the individual lines coupled to each controller. The controllers are shown in more detail in FIG. 2. Each controller includes a buffer and latch 41 coupled through line 43 to microprocessor 29. The processor 29 is coupled through an address decoder 69 to buffer 41 and to a memory consisting of dynamic RAM 40, static RAM 38, and EPROM 37. The processor 29 is also coupled through line 46 to a memory page control 39. The processor 29 is coupled through line 44 directly to the dynamic RAM 40, static RAM 38, and eprom 37. Coupled to the static RAM 38, is a standby power block 30 which provides battery backup during power failure. The clock receiver is coupled to the clock bus 22, switching element 32 and interface element 33. Power is supplied through a DC voltage regulator 34 and a power up/down circuit 31 provided on each controller sequences the activation and deactivation of the microprocessor 29, the SE 32, and the static RAM 38. The switching element 32 is coupled to th interface element 33. The interface element is coupled to the Xbus 23 through a transceiver 36. The interface element 33 is also coupled to digital station interfaces and to analog device interfaces through serial data bus 42, link/codec select line 79, and link control signal line 71.

Detailed Description Text - DETX (176):
The processor buffer consists of a double buffering scheme which is similar to the link/codec buffer and Xbus buffer. The buffer consists of two buffers 54A and 54B with each having an input portion and an output portion. These buffers are memory mapped into the address space of the processor 29 so that the real time code has access to one of the buffers at a particular time while the SEP 64 will process information in the other buffer. The processor 29 access and SEP 64 switch buffers every millisecond (superframe). This means that every 125 microseconds only one byte of link control information and one byte of intercontroller information is swapped. A total of one millisecond is

United States Patent [19]

Burns et al.

[11] **Patent Number: 4,791,629**

[45] **Date of Patent: Dec. 13, 1988**

[54] **COMMUNICATIONS SWITCHING SYSTEM**

[75] Inventors: C. A. Burns, Palo Alto, Calif.; Calvin H. DeCoursey, Reno, Nev.; Hans H. Jordan, Mountain View, Calif.

[73] Assignee: IBM Corporation, Santa Clara, Calif.

[21] Appl. No.: 859,380

[22] Filed: Jan. 2, 1986

[51] Int. Cl.[4] H04J 3/16

[52] U.S. Cl. 370/88; 370/95

[58] Field of Search 370/88, 95, 89, 86, 370/94, 110.1, 67

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,548,231	10/1985	Ke Nodin et al.	370/89
4,621,284	12/1986	Brown	370/85
4,630,261	12/1986	Townsend et al.	370/85
4,663,758	5/1987	Lazzarelli et al.	370/85

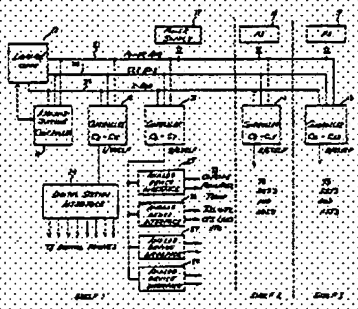
Primary Examiner—Douglas W. Olms

Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

A communication switching system in which control functions are distributed homogeneously, as opposed to being distributed by individual function, throughout the system. A plurality of controllers are coupled to a time division multiplex (TDM) bidirectional bus. Each controller includes a microprocessor to perform control functions. An interface element on the controller accesses the TDM bus while a switching element on each controller controls access between the interface element and the microprocessor. The switching element and interface element include storage areas which are double buffered to allow for more efficient operation and use of the memory space. The TDM bus is divided into a plurality of time slots. Each controller is assigned certain of the time slots and utilizes those time slots to communicate with other controllers. The system includes provisions for dynamic allocation of time slots.

16 Claims, 15 Drawing Sheets



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Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1. Document ID: US 6381674 B2

L1: Entry 1 of 6 File: USPT Apr 30, 2002

US-PAT-NO: 6381674
DOCUMENT-IDENTIFIER: US 6381674 B2

TITLE: Method and apparatus for providing centralized intelligent cache between multiple data controlling elements

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 5790775 A

L1: Entry 2 of 6 File: USPT Aug 4, 1998

US-PAT-NO: 5790775
DOCUMENT-IDENTIFIER: US 5790775 A

TITLE: Host transparent storage controller failover/failback of SCSI targets and associated units

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 5630169 A

L1: Entry 3 of 6 File: USPT May 13, 1997

US-PAT-NO: 5630169
DOCUMENT-IDENTIFIER: US 5630169 A

TITLE: Apparatus for a host central processor with associated controller to capture a selected one of a number of memory units via path control commands

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 4. Document ID: US 5530845 A

L1: Entry 4 of 6 File: USPT Jun 25, 1996

US-PAT-NO: 5530845
DOCUMENT-IDENTIFIER: US 5530845 A
** See image for Certificate of Correction **

TITLE: Storage control subsystem implemented with an application program on a computer

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

5. Document ID: US 5504926 A

L1: Entry 5 of 6 File: USPT Apr 2, 1996

US-PAT-NO: 5504926
DOCUMENT-IDENTIFIER: US 5504926 A

TITLE: Method for a host central processor and its associated controller to capture the selected one of a number of memory units via path control commands

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

6. Document ID: US 4791629 A

L1: Entry 6 of 6 File: USPT Dec 13, 1988

US-PAT-NO: 4791629
DOCUMENT-IDENTIFIER: US 4791629 A

TITLE: Communications switching system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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4791629.pn. or 5504926.pn. or 5530845.pn. or 5630169.pn. or 5790775.pn. or 6381674.pn.	6

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